DDS with Noise Reduction by Multiplier-Less Filter Methods

1st Stefan Jahn
University of Applied Sciences Upper Austria
Softwarepark 11, 4232 Hagenberg, Austria
stefan.jahn@students.fh-hagenberg.at

2nd Hans-Georg Brachtendorf
University of Applied Sciences Upper Austria
Softwarepark 11, 4232 Hagenberg, Austria
hans-georg.brachtendorf@fh-hagenberg.at

***Abstract*—Direct Digital Synthesizers have the disadvantage, that they need for a better spurious free dynamic range (SFDR) a greater bit width to reduce the uniformly distributed white noise caused by the quantization. This leads to large look up tables, or when methods of noise shaping effects are used, to even larger sizes of the table. So it is necessary to make a trade-off between memory usage and resulting signal quality. This paper focuses on the reduction of the size of the look up table and reducing the resulting higher noise floor by the combination of multiplier-less digital filters, noise shaping and dithering. The advantage of multiplier-less filter implementations are higher clock rates, smaller dial spaces, and on FPGA implementations the usage of DSP blocks is avoided, which can be limited on smaller fabrications. As final output, this work provides a MATLAB test and design environment followed by a VHDL implementation inclusive testbench.**

***Index Terms*—Direct Digital Synthesizers, DDS, Noise Shaping, CIC Filter, Multiplier-Less Filter**

I. Introduction

Due to the rapid development of electronic devices with radio frequency capabilities it is mandatory to improve the generation of sinusoidal signals with the ability of quick changes in frequency and/or phase. The approach of direct digital synthesizers (DDS), firstly introduced in [2] fits perfect into those requirements. Since this is a digital approach, the resulting signal has additional noise caused by quantiazation of the look-up table (LUT), the phase accumulator (ACC) and as well from some other sources, described in [3]. To get partly rid of these effects, current DDS processing chains additionally employ noise shaping (NS) by digital filtering to shift the noise near the desired frequency into unused bandwidths. The disadvantage of this approach is, that the bitwidth of the LUT must be increased, to obtain a signal where the intrinsic noise floor is lower, which can then be shaped. An example of this structure can be seen in Figure 1, with the accumulator bitwidth k (LUT addresses), the LUT entry bitwidth $m+x$ and the resulting output/DAC bitwidth m. In [3] there is also a system described where the phase accumulator output is shaped by the noise shaping filter, but this is out of scope of this paper.
In the following a DDS system with an additional multiplier-less filter method is described. With this approach the mean energy of the noise floor can be reduced without an increase of the bitwidth of the LUT.

II. Advanced DDS Concept

By adding a filter in the processing chain, as seen in Figure 2 the noise floor can be reduced without an increase of the LUT's bitwidth. To improve the design without a proper increase in area and memory usage, multiplier-less filter methods must be aimed at. This can be done by the usage of cascaded integrator comb filters (CIC filter) [4]. But this sort of filter has the disadvantages of a deficient stopband suppression (about -13dB) when used in the first order form and the poor transition from pass- to stopband, which gets worse on higher order filters. Another approach is to use a higher order CIC filter solved by backward differential formulas (BDF filter) [5] [6]. This sort of filter has a steeper transition from stopband and passband, but with the drawback, that the stopband suppression is not that good compared to an equal order CIC filter. Last step of the new DDS concept is to reduce the bitwidth of the filtered signal to the desired bitwidth used in the DAC by a noise shaping filter. This must be done, because the bitwidth growths by the usage of CIC or BDF filters, since the latter ones are a modified form [4].

III. Multiplierless BDF Filter

As described in [6] the transfer function of a BDF filter is given by

$$H_{BDF}(z) = \frac{2}{D^2} \cdot \frac{1 - z^{-D}}{1 - z^{-1}} \cdot \frac{3 - 4z^{-\frac{D}{2}} + z^{-D}}{3 - 4z^{-1} + z^{-1}} \qquad (1)$$

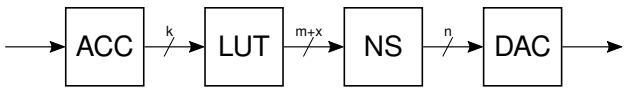

Fig. 1. Classic DDS Structure

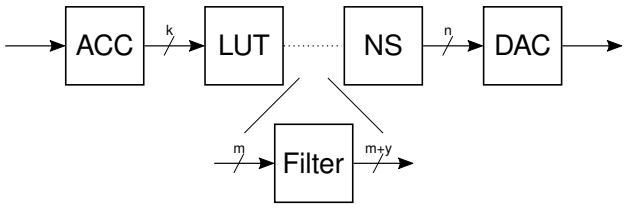

Fig. 2. Advanced DDS Structure

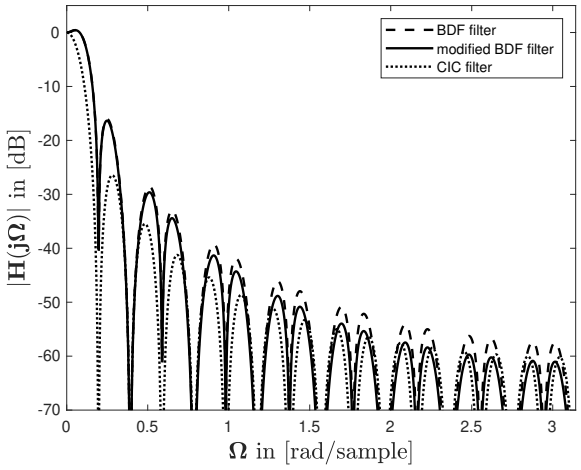

Fig. 3. Comparison of the presented filter types in second order form, where Ω is the normalized frequency ($\Omega = 2\pi f/fs$) in radiant per sample.

where D is the filter delay. But on looking at the third fraction, there is a factor with the value $\frac{1}{3}$. This factor can neither be implemented multiplier-less, nor can it be represented by any fixed point number.

But this problem can be simply solved by splitting up the denominator of the third fraction into $(1-z^{-1})\cdot(3-z^{-1})$ and moving the pole from $p = \frac{1}{3}$ to the position $p = \frac{1}{2}$. Due this shift, additional scaling of the transfer function must be done. This results into the modified BDF filter transfer function given by

$$H_{BDF}(z) = \frac{1}{D^2} \cdot \frac{1-z^{-D}}{1-z^{-1}} \cdot \frac{3-4z^{-\frac{D}{2}}+z^{-D}}{(1-z^{-1})\cdot(2-z^{-1})}. \quad (2)$$

In Figure 3 the differences between the modified BDF filter, the BDF filter from [6] and a second order CIC filter are shown. As can be seen, the magnitude response of the modified BDF filter has the same pass- to stopband transition and even a slightly better stopband suppression.

IV. Implementation Aspects

A. BDF Filter

Furthermore, the DDS system must be capable to generate signals in a wide frequency range. But as can be seen in Figure 3 the passband of the BDF filter with a delay (D) of 32, has only a bandwidth of about 0.12Ω, until the -3dB threshold has been reached. To increase the range of synthesizeable frequencies, the delay can be decreased to the next lower power of two factor when the -3dB threshold gets reached. In Figure 4 the magnitude responses of BDF filters with different delays (from 64 down to 2, in power of two steps) are shown. The horizontal line at -3dB represents the switching border. As can be seen, the lower the delay, the poorer the stopband suppression. So the best results are achieved at lower frequency ranges. For the final DDS system in this paper, the delays from 64 downto 4 are selected, because a delay of 2 does not improve the range of the synthesizeable frequencies. This setup leads to a range from DC to about $0.72radpersample(rad/s)$.

During simulation also a stability issue arised, on switching between frequencies, which use different filter delays. This can be resolved by resetting the memory of the filter on a delay switch. But this has the drawback of loosing the advantage of phase continuity.

B. Noise Shaping

As mentioned before, the final frequency range is from DC to $0.72rad/s$, thus the noise shaping filter must only implement a highpass filter [3] [7]. This can either be the transfer function $G(z) = 1 + H(z) = 1 - z^{-2} + z^{-1}$ or $G(z) = 1 - z^{-1}$. In comparison, the first one has a better suppression of the low frequency parts, but the high frequency parts have a greater amplification than the second one (difference of about 6dB), as seen in Figure 5.
Finally in this paper, the second noise shaping filter function has been implemented, because of the BDF filtering, the noise near the desired frequency is not suppressed. This leads to very small quantization errors, thereby the noise shaping has on thus frequencies no effect, so a magnitude response with less amplification of the high frequency parts is more beneficial.

C. Dithering

To improve the signal further with less additional effort, the method of dithering is used inside the noise shaping structure to linearizize the quantization error of small amplitude errors, as described in [7]. As dither source a pseudo-noise sequence implemented as a linear feedback shift register (LFSR) is used [8]. Advantage of this implementation is the simplicity, but with the disadvantage, that the spectrum of the generated numbersequence is not uniformly distributed (white noise), but the difference is very small, so in this application it can be neglected. For generating this random number a 24 bit polynom in the form

$$p(x) = x^{24} + x^{23} + x^{22} + x^{17} + 1 \quad (3)$$

is used [8].

V. Matlab Simulation Results

A. General

Within this paper, a *MATLAB* environment for designing and testing the described DDS structure also gets published. These scripts are fully bit true, so the results can be achieved on any functional hardware platform.
The following results shown in this paper are with the parameters/bitwidths presented in Table I, where *k* is the bitwidth of the accumulator, *m* the bitwidth of a look up table entry, *n* the bitwidth of the digital to analog converter, *m+y* the bitwidth of the BDF filter output and *q* the BDF filter internal bitwidth (see Figure 2). The sampling frequency used for the plots is $fs = 1$ MHz.

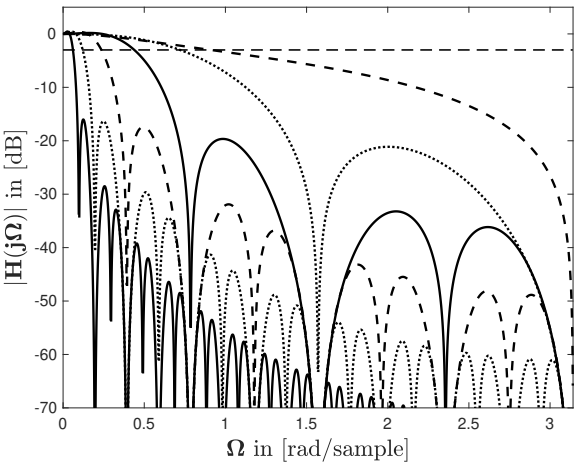

Fig. 4. BDF filters with delays from 64 down to 2.

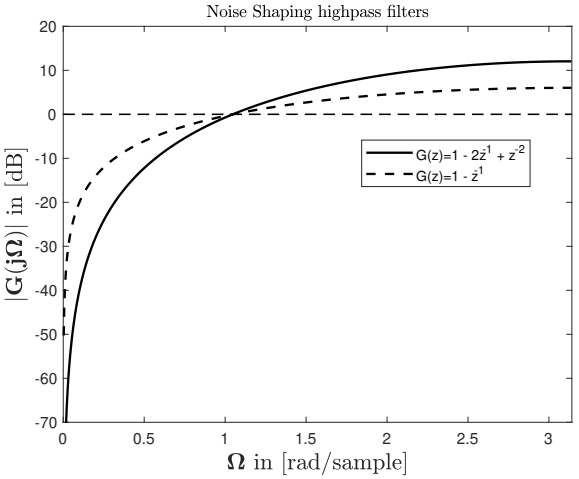

Fig. 5. Noise Shaping highpass filters.

B. Spectral results

In Figure 6 and 7 the relative spectral power density of two synthesized frequencies (10kHz and 20kHz) of the new DDS structure are shown. As can be seen, the resulting signal quality of the synthesized 10kHz signal with less memory usage reaches almost the same noise floor as the reference signal with a LUT bitwidth of 16 bits (shown in figure 8). Only the noise floor around the generated signal is not that good, due the bandwidth of the BDF filter. On looking at the generated signal with a frequency of 20kHz it can be seen,

parameter	**bitwidth**	fixed format	block
k	12	12.0	ACC
m	8	0.7	LUT
m+y	20	0.19	BDF filter
q	22	2.19	BDF filter
n	16	0.15	DAC

TABLE I
SIMULATION PARAMETERS

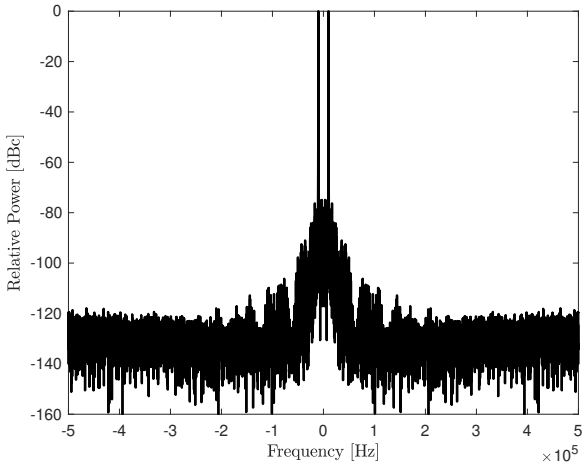

Fig. 6. 10kHz signal with a LUT width of 8 bits and a resulting bitwidth of 16 bits, achieved by BDF filtering and noise shaping.

that the noise floor around the desired frequency gets worse the lower the delay of the BDF filter is. But the overall noise floor is still near the -120dB area from the reference signal.

C. Theoretical memory improvement

With this setup, it is theoretically possible to save a minimum of about 32% memory compared to a DDS system with a LUT of 16 Bits, when it is implemented as a quarter table. This means, that the LUT stores only the first quadrant of the sinus entries, since the other quadrants can be represented due the symmetric properties of a sinusoid signal (mirroring and sign change). Finally this results in a memory usage of 11094 bits, where 8192 bits are used in the LUT, 2882 bits in the BDF filter and 20 bits in the noise shaping structure, compared to 16384 bits memory on an implementation with a LUT wordlength of 16 bit. This memory reduction can even be pushed further due some implementation tweaks discussed in the next section.

VI. VHDL Implementation / HDL Implementation / Hardware Implementation and Results

A. General

As mentioned, the whole system has been implemented in VHDL93 with the addition of generating a sinus and a cosinus signal, which leads to a doubled size of the BDF filter and noise shaping structure, since they are neccessary for each of the two signals. For testing and verification the open source tools *GHDL* and *cocotb*, and as synthese tool Quartus Prime Lite Edition v20.1, has been used. As target platform, the Altera Cyclone V FPGA has been used.

B. BDF Filter Implementation

In Figure 9 the blockdiagram of the BDF filter transfer function given by Equation 2 is shown. The first row of the blockdiagram represents the numerator (comb filters) with the gain, where each single delay block is implemented as

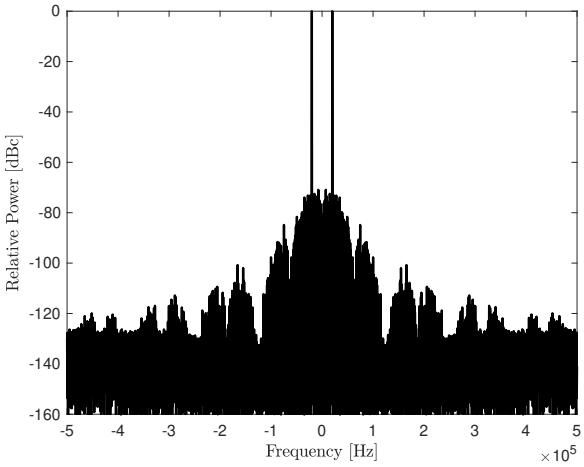

Fig. 7. 20kHz signal with a LUT width of 8 bits and a resulting bitwidth of 16 bits, achieved by BDF filtering and noise shaping.

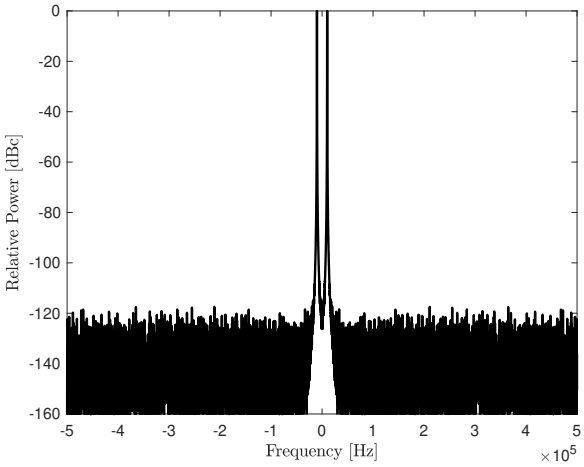

Fig. 8. 10kHz signal with a LUT width of 16 bits and no further processing (reference).

a RAM, and the second row the denominator (integrators), where the delay blocks are implemented as registers. In this representation it can bee seen, that the delay chains of the comb filter parts do not need the full internal bitwidth of 22 bits (given by Table I), since the first delay chain operates only with the input signal, wich has 8 bits. The second and third delay chains operate with a signal, wich is built by a 8 bit addition, which results in 9 bit and a rightshift by $\log_2(D)$. But the rightshift can also be put after the comb structure (next to the other rightshift). So the second and third delay chains need a bitwidth of 9 bits (input bitwidth + 1). But by doing this, the bitwidth of the combinatoric inside of the second comb filter must be increased by 4 bits (two addtions and one leftshift by 2), to ensure that no overflow can happen.

	conventional DDS		advanced DDS	
	Memory Bits	**Register Bits**	**Memory Bits**	**Register Bits**
ACC	0	25	0	25
LUT	15360	34	7168	18
BDF	n.a.	n.a.	2176	300
NS	n.a.	n.a.	0	100
Total	**15360**	**59**	**9344**	**443**

TABLE II
SYNTHESE RESULTS OF THE CONVENTIONAL DDS AND THE ADVANCED DDS SYSTEM WITH QUADRATURE SIGNAL GENERATION

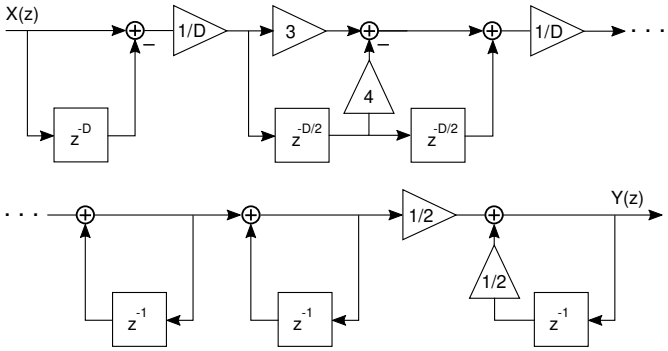

Fig. 9. Blockdiagram of the implemented BDF filter, where the delay D can be dynamically adapted.

C. Results

VII. Conclusion and further work

Acknowledgment

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